

# Efficient power consumption encoding technique for DSRC applications

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## ABSTRACT

The emerging technique nowadays in communication is very vast. Applications relating to communication in general are co related with one another. There is a critical need in communication systems in order to avoid various interferences occurring in modern communication. The aim of the paper presents to achieve dc balance and signal reliability in communication. DSRC adopts FM0/Manchester code basically to achieve the aim but in addition to it miller code has been introduced to reach well efficient power consumption. SOLS technique is adopted in order to overcome the limitations proposed by FM0/Manchester code. The proposed method competes improvement in power consumption due to miller encoding. Thus in no way not wanting to limit the work of communication this paper has been enhanced to combat with various encoding techniques. Therefore institutional structures of broadcasting are large and so communication is the basic need of it.

**KEY WORDS:** Fm0, Manchester, Miller Encoding, SOLS.

## 1. INTRODUCTION

The DSRC system is an important communication method. The proposed description of the paper starts with a basic encoding technology such as binary bits. The processing includes three encoding forms namely fm0/Manchester and miller. Generally DSRC architecture includes baseband processing, Frontend. The system is based on baseband processing wherein it ensures about the encoding techniques (Ahmed- Zaid, 2011). At a certain point, however, the broadcasting structures must yield encoded messages in the form of a meaningful discourse. The production process is not without its 'discursive' aspect: it, too, is framed throughout by meanings and ideas. The message form is sent in order of sending message and then followed by receiving message. Baseband processing includes encoding, synchronization and hence it has been adopted. The SOLS technique which is used can be of efficient in reducing the area thereby reducing transistor count (Benabes, 2003). The paper puts forth achievement in enhancing communication reliability.

### Theoretical Background

**Fm0 Principles:** FM0 is also known as Biphas space encoding. They include the basic principles for transition so the transition inhibits the principles where it follows the logic of 0, 1 transition. Transmission is from one end of the processor and completes the cycle to given logic. FM0 encoding contains sufficient data to recover clock data forms.

- If the input is the logic-0 FM0 code must exhibit a transition between A and B.
- If the input is the logic-1, no transition is allowed between A and B.
- The transition is allocated among each FM0 code no matter what the X is.

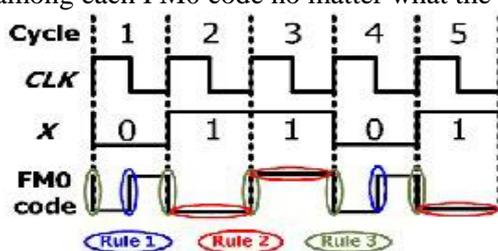


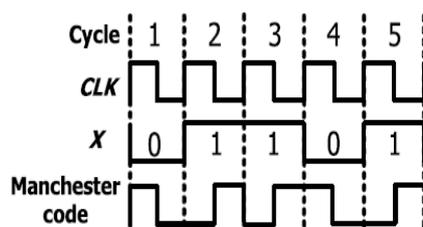
Figure.1. Fmo encoding

In FM0 encoding, a transition is present on every bit cell boundary, and an additional transition may be present in the middle of the bit cell. In FM0, a 1 bit is sent as no transition in the centre of the bit cell, and a 0 bit is sent as a transition in the centre of the bit cell.

## 2. METHODS AND MATERIALS

**Manchester Principles:** Manchester encoding is also called phase encoding. Manchester is used for a higher operating frequency. Manchester encoding is a very common method and are used often. The signals of Manchester are transmitted serially. In Manchester encoding the average power is always the same, no matter what data is transmitted.

- The Manchester code is based on the logic  $X \oplus CLK$ .
- The XOR operation is used for realization of the operation of CLK and X.
- Since the clock always has a transition within one cycle and so does the Manchester code no matter what the X is.



**Figure.2. Manchester Encoding**

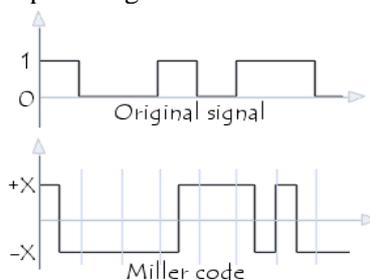
Manchester code follows an algorithm to encode the data. It always produces a transition at the center of the bit. It contains sufficient information to recover a clock. So if the data rate is twice, sufficient clock information can be recovered from the data stream so that separate clocks are not needed.

### Proposed System

**Description of Miller Encoding Technique:** Miller encoding is also known as delay encoding so is used for higher operating frequency and it is similar to Manchester encoding except that the transition occurs in the middle of an interval when the bit is 1. Hence by using the miller delay, noise interference can be reduced.

- Miller encoding, is similar to Manchester encoding.
- Except that a transition occurs in the middle of an interval only when the bit is 1.
- This allows higher data rates.

So, when it requires transition at input logic-1 means we must use the Miller encoding technique, because transition occurs in Miller code when the input is logic-1 and no transition occurs when input is logic-0.



**Figure.3. Miller Encoding**

In Fm0 encoding technique the transition occurs only when input value is logic-0. No transition occurs when input value is logic-1. But in miller it is not that case.

### 3. RESULTS AND DISCUSSION

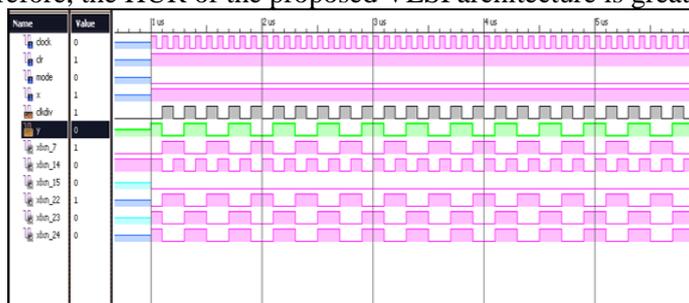
This paper is compared with the existing articles these articles are implemented in two kinds of design flows. The literatures are realized with full-custom and the literatures are designed with FPGA. To give an objective evaluation, the proposed VLSI architecture is realized with both design-flows, as listed in comparison table below. The main advantage is that the signal synchronizes itself, minimizes the error rate, and optimizes the reliability. The drawbacks to this encoding are that more bits are needed to transmit in the Manchester encoding signal than the original signal, and it needs more bandwidth.

**Table.1. Comparison of Miller, Manchester and Fm0 Encoding**

Encoding	Minimum Pulse Width	No Of Transition	Normalized Average
Miller	$T_b$	5	3.5/8
Manchester	$T_b/2$	11	1/2
Fm0	$T_b/2$	12	4.5/8

**Comparison with Sophisticated Articles:** This paper adopts the proposed sol's technique to construct a fully reused vlsi architecture for both fm0 and manchester encodings. Every logic component of this design is not only used in fm0 encoding, but also in Manchester encoding. None of them is wasted in either encoding function; therefore, the hur of the proposed VLSI architecture is as high as 100%. The performance evaluation classifies the electrical characteristics into the operation frequency, the power consumption, and the area. They are all normalized to 0.18  $\mu\text{m}$  for an objective evaluation for manchester encoding, the operation frequency of this paper is comparable with that of but slower than that of the literature is dedicated to optimize the signal path by reducing the number of transistors, and thereby has faster operation frequency. The adoption of FM0 or Manchester code depends on Mode and CLR. In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller. Whether FM0 or Manchester code is adopted, no

logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved.



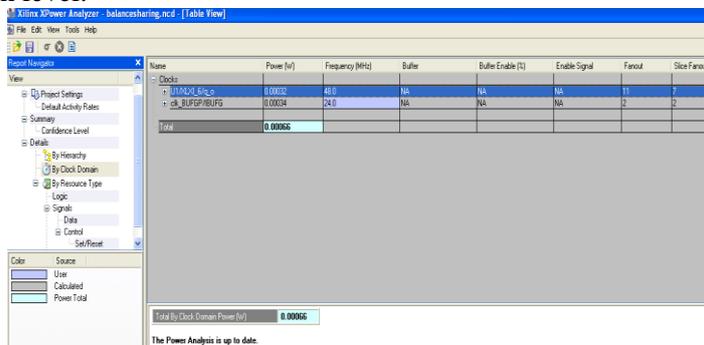
**Figure.4. Simulated Waveform of Existing System**

The FM0 encoding for the RTL Schematic is done in a behavior style using verilog. The functioning of the schematic is implemented using the state parameters as clock and input data, gates, FF, and MUX. The above schematic uses very little hardware and also minimizes the complexity.



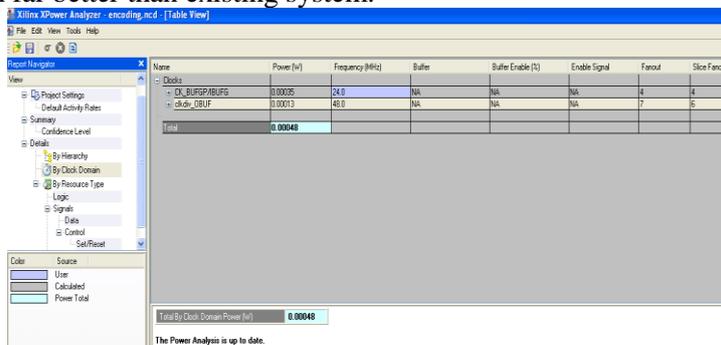
**Figure.5. Simulated Waveform of Proposed System**

The Miller encoding of the RTL schematic is done in a behavior style using verilog. The function of the schematic is implemented using the state parameters as clock and input data, TFF, DFF, and gates. The schematic in Figure has an easy transition level.



**Figure.6. Power Consumption of Proposed System**

The existing encoding is less efficient and not much of power is being consumed so it has to be improved with techniques that is more efficient when comparing with other techniques hence miller encoding is introduced and its power consumption far better than existing system.



**Figure.7. Power consumption of existing system**

The power consumption of proposed system has an improvement in comparison with the existing system therefore it has greater consumption quality over other encoding techniques.

**4. CONCLUSION**

A new technique called miller technique has been introduced to enhance the existing work. Therefore the encoding capability can fully support the DSRC standards. Thus the paper not only supports DSRC but also exhibits a competitive performance in comparison with existing work. This work can also be enhanced in future with further improvement in power and area also. They can be implemented in Spartan6 board.

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